INTERIM ENGINEERING REPORT

NO. 1

INTEGRATED CIRCUIT STUDY

64-5

This report covers the period 1 June thru 31 August 1963

U N I V A C

DIVISION OF SPERRY RAND CORPORATION

UNIVAC PARK, ST. PAUL 16, MINNESOTA

NAVY DEPARTMENT
NObsr 89341

BUREAU OF SHIPS

September 1963

ABSTRACT

This report describes the progress achieved in the integrated circuit study program for the GP-667 Computer.

Significant accomplishments were recorded in the following areas: selection of a circuit type and performance testing of existing available integrated circuits.

PART I

PART I

Section 1

PURPOSE

This study is intended to compare monolithic integrated circuits, capable of performing in the CP-667 Computer, with the present hybrid (multiple chip) micro circuits per MIL-M-23700/1 thru 5.

Electrical performance, functional stability and reliability are to be evaluated.

PART I

Section 2

GENERAL FACTUAL DATA

IDENTIFICATION OF PERSONNEL

The following list summarizes the personnel actively working on the project for each month during the period of this report:

PERSONNEL	JUNE (160 Hrs.)	JULY (200 Hrs.)	AUGUST (160 Hrs.)
Granberg	0	5	15
Janisch	0	0	38
Magnuson	0	0	1
Schipp	0	0	1
Sundem	0	6	24
Wheeler	0	0	1
Wozniczka	0	24	108

PART I

Section 3

DETAILED FACTUAL DATA

SELECTION OF CIRCUITS

The logic circuitry of the CP-667 is made up of nine printed circuit card types described in Table I. The circuits on these cards are developed by interconnecting the hybrid (multiple chip) circuits of MIL-M-23700/1,2,3,4,5.

Integration of the hybrid circuits suggests the combination of the diode gate and transistor gate in one package so as to provide for connection of the substrate to the most negative potential. A minimum number of integrated circuit types are desirable to keep the tooling and testing practical. The complexity of the circuitry in any one package is limited by the number of external connections. Table I provides a breakdown of three likely circuit groups employing ten external connections. The number of circuit packages required to duplicate a given card function is compared with the presently used hybrid packages. The use of external collector resistors, and performing the "or" function at the collectors were factors in this summary.

The optimum circuit group in terms of simplicity and versatility is the 3/3 and 2/4 input combination. This is particularly desirable in view of one vendor's suggestion that the basic chip could be made with 4 input diodes on each circuit enabling either package to be made from the same chip by merely changing the final connections to the terminals.

The specification for the procurement of a 3/3 integrated circuit is attached. Subminiature resistor packages are being investigated for use as collector resistors for these circuits. This provides an option of performing the "or" function at the collector and minimizes heat dissipation within the integrated circuit.

A complementary transistor logic gate utilizing a PNP/NPN combination on one integrated chip has recently been suggested as a possible substitute for the diode gates of MIL-M-23700/1 thru 4. This system could ideally permit logic (and/or functions) to be performed without inversion at the base of the inverter circuit (MIL-M-23700/5). This phase of the program requires more circuit research before specification and procurement can be initiated.

PRELIMINARY STUDIES

Westinghouse type 2201 integrated Diode Transistor Logic (DTL) circuits were tested in the circuit of Figure 1. The series string was driven by and loaded with a CP-667 hybrid circuit. Figure 2a shows waveforms at each node in this configuration when no collector resistors, R_c, were used with the 2201 circuits. Figure 2b illustrates the waveforms at the same nodes with 400 ohm collector resistors. Propagation times (measured from 10% of final voltage level of the input to 10% of the final voltage level of the output) through each of the stages are summarized below:

NODE	$R_c = \infty$		R_c = 400 OHM	
	TURN ON	TURN OFF	TURN ON	TURN OFF
II	17 ns	17 ns	12 ns	8 ns
III	46	16	16	26
IV	42	20	16	18
V	40	12	15	20

It should be noted that this represents a best case condition since the fan-out was unity and nominal conditions existed. The waveshape of the present hybrid CP-667 circuit (Node I) has a much faster rise and fall time than that of the integrated 2201 circuits. This can be attributed to the absence of parasitics in the hybrid circuits and the higher power level of the circuit.

An existing UNIVAC integrated logic circuit was wired in a series string driven by and driving a CP-667 hybrid circuit as shown in Figure 3. Figure 4 shows the waveforms at each node in the configuration. Propagation times (10% to 10% levels) for each node are shown below:

NODE	TURN ON	TURN OFF
II	12 ns	30 ns
III	33	30

Again note that the waveshape of the CP-667 hybrid circuits was superior to that of the tested parts. This sharp rise time accounts for the fast turn on of Node II. This circuitry is slower than the 2201 circuitry when operated with a collector resistor.

PART I

Section 4

CONCLUSIONS

The preliminary studies of two types of integrated circuits indicate that speeds in the range required for the CP-667 are possible from integrated circuits when operated at the same power level. The "or" function must be performed at the collector rather than the bases in order to minimize the base overdrive and subsequent increase in storage time.

PART II

PART II

PROGRAM FOR NEXT QUARTER

1. Procure hybrid circuits for comparison with integrated devices.

2. Arrange to procure from two manufacturers of integrated circuit samples of the 3/3 DTL circuit described in the attached specification.

3. Perform exploratory testing of the Complementary Transistor Logic Gate and prepare procurement specification for this circuit.

4. Procure samples of subminiature resistor package for use as collector resistors.

5. Establish an environmental test program designed to most efficiently determine modes of failure and degradation of characteristics.

PART III

SUPPLEMENTARY DATA

CARD ASSEMBLY	CARDS PER 667 MACHINE	CARD FUNCTION	CIRCUIT PACKAGES REQUIRED TO PROVIDE CARD FUNCTION						
			PRESENT CP-667 (HYBRID)	PROPOSED INTEGRATED GROUPS					
				GROUP 1	GROUP 2			GROUP 3	
				3/3 CIRCUIT	22/2	3/3	7	3/3	2/4
4224000	143	22/22/22/22	5	4	3			4	0
4224010	127	333/334	4	NOT POSSIBLE		3	1	3	1
4224020	138	3/4/3/4	4	NOT POSSIBLE		1	2	1	2
4224030	155	2222/2222/2222	7	6	4			6	0
4224040	349	2/2/2/2/2/2/1	5	3	3			3	0
4224050	111[1]	8/8	3	NOT POSSIBLE			2[2]		4[3]
4224060	97	22222/22222	6	5	4			5	0
4224070	246	FF - 2222S 12C/2222S 12C	8	8	6			8	0
4224080	467[1]	FF - 33S 3C/33S 3C	7	5	2	3		5	0

1 — 72 of these for memory
2 — Input reduced by one
3 — At reduced speed

TABLE I

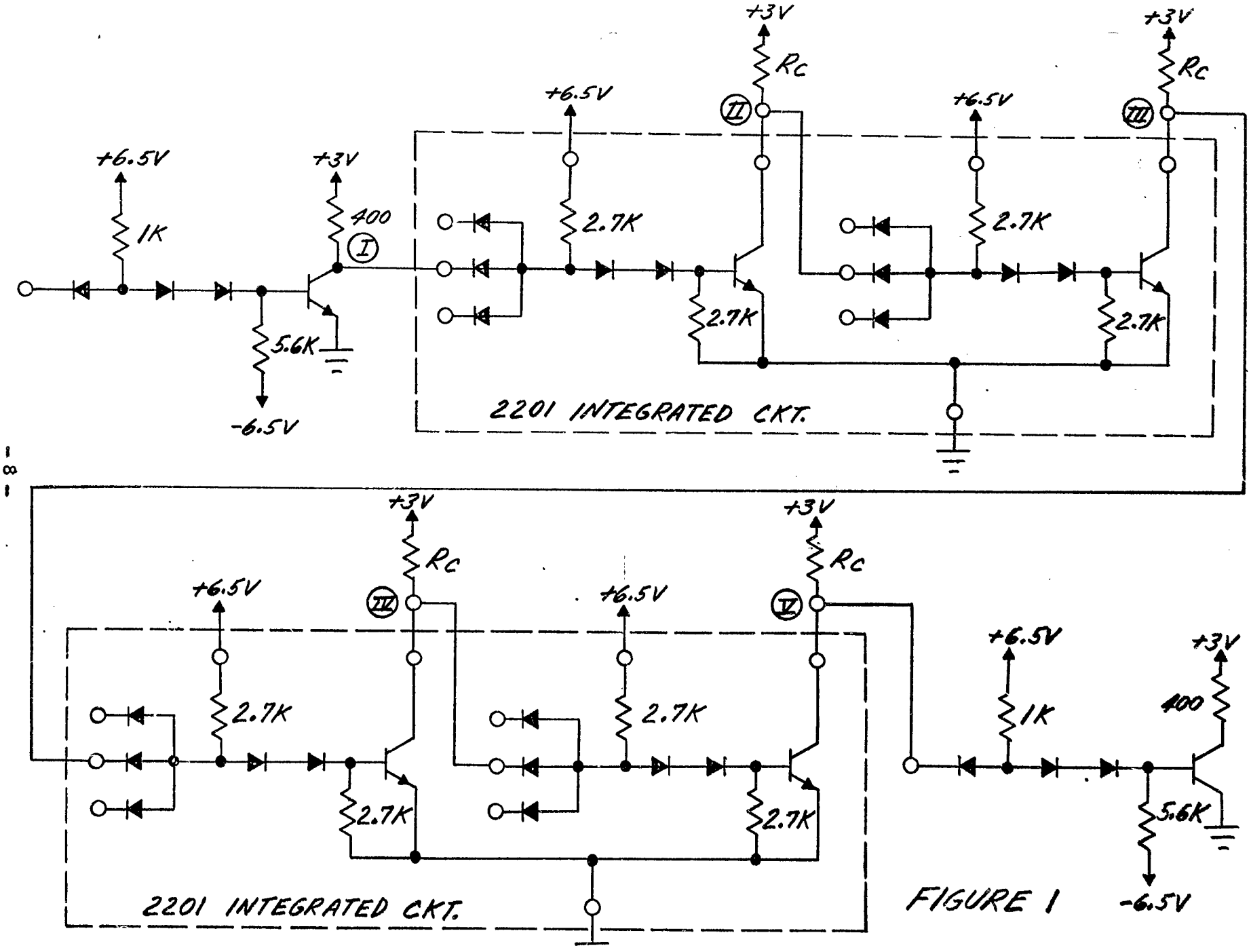

+6.5V
1K
+3V
400
I
5.6K
-6.5V
+6.5V
2.7K
2.7K
+3V
Rc
II
+6.5V
2.7K
2.7K
+3V
Rc
III
2201 INTEGRATED CKT.
+3V
Rc
III
+6.5V
2.7K
2.7K
+3V
Rc
IV
+6.5V
2.7K
2.7K
2201 INTEGRATED CKT.
+6.5V
1K
+3V
400
5.6K
-6.5V

FIGURE 1

CALIBRATION: Vertical - 1 volt/square
Horizontal - 25 ns/square

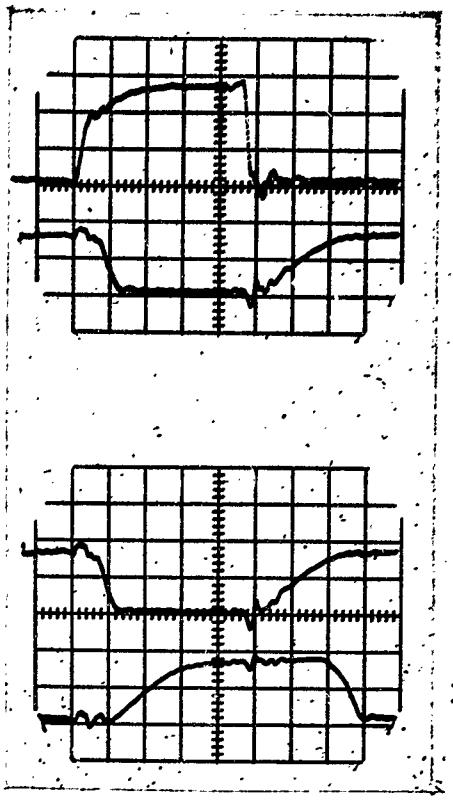


FIGURE 2a.

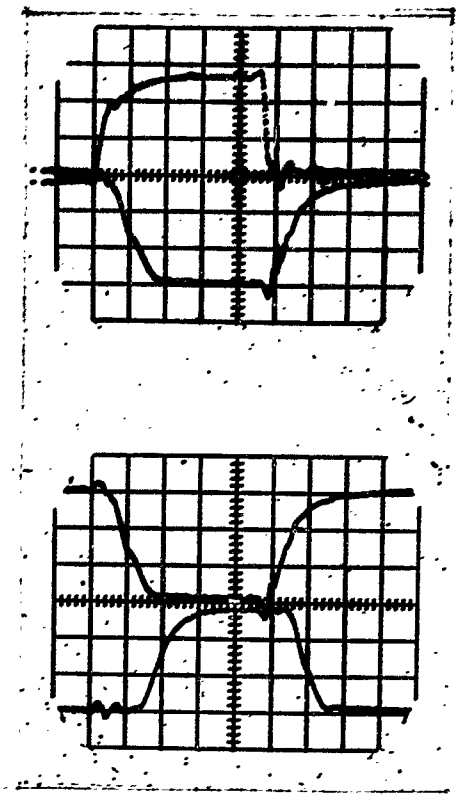


FIGURE 2b.

WAVESHAPES-INTEGRATED DTL

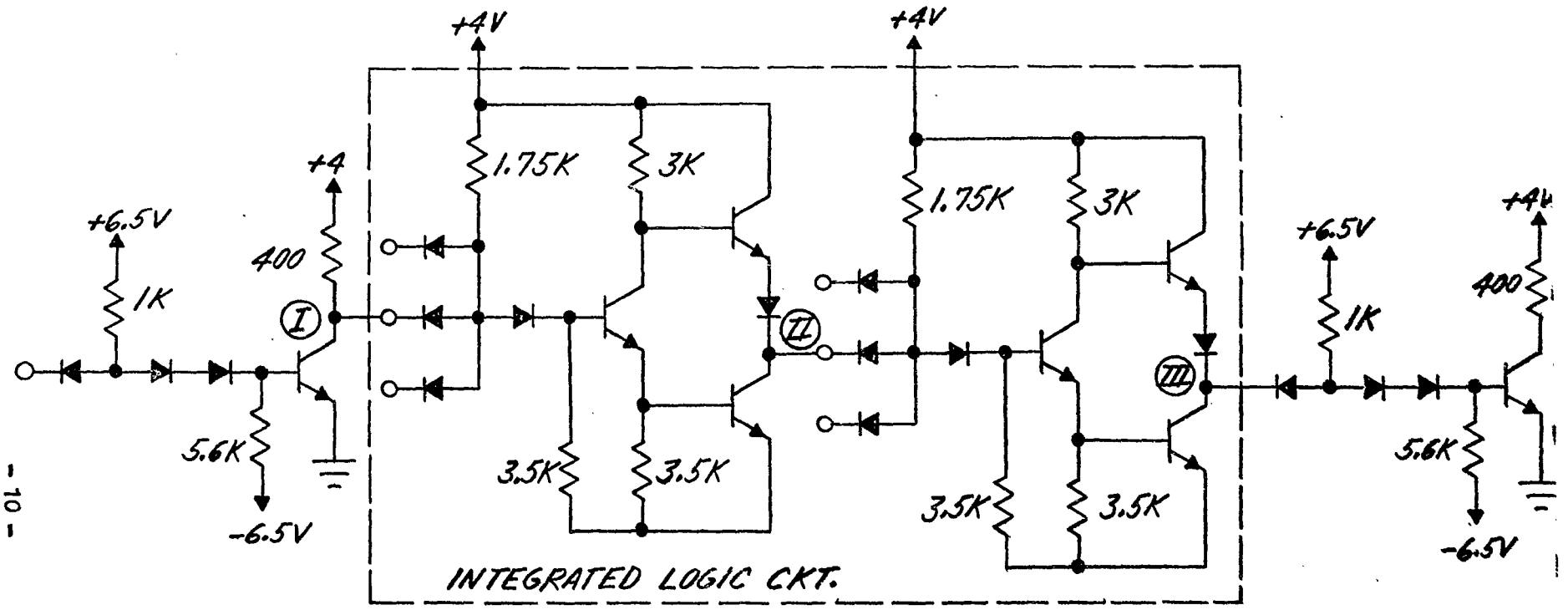

+4V
+4V
+4
+6.5V
400
1K
5.6K
-6.5V
1.75K
3K
3.5K
3.5K
I
II
III
INTEGRATED LOGIC CKT.

FIGURE 3

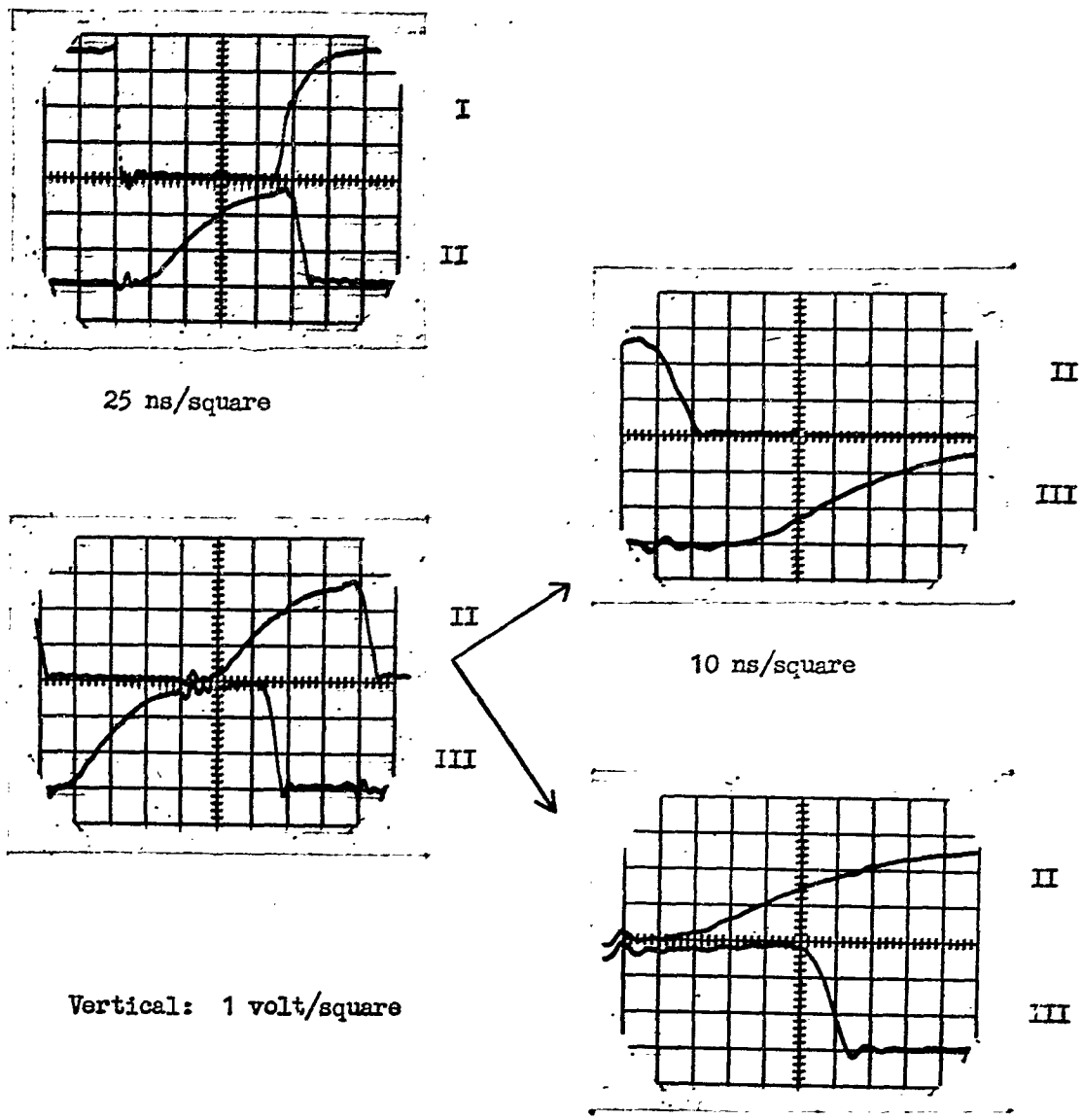
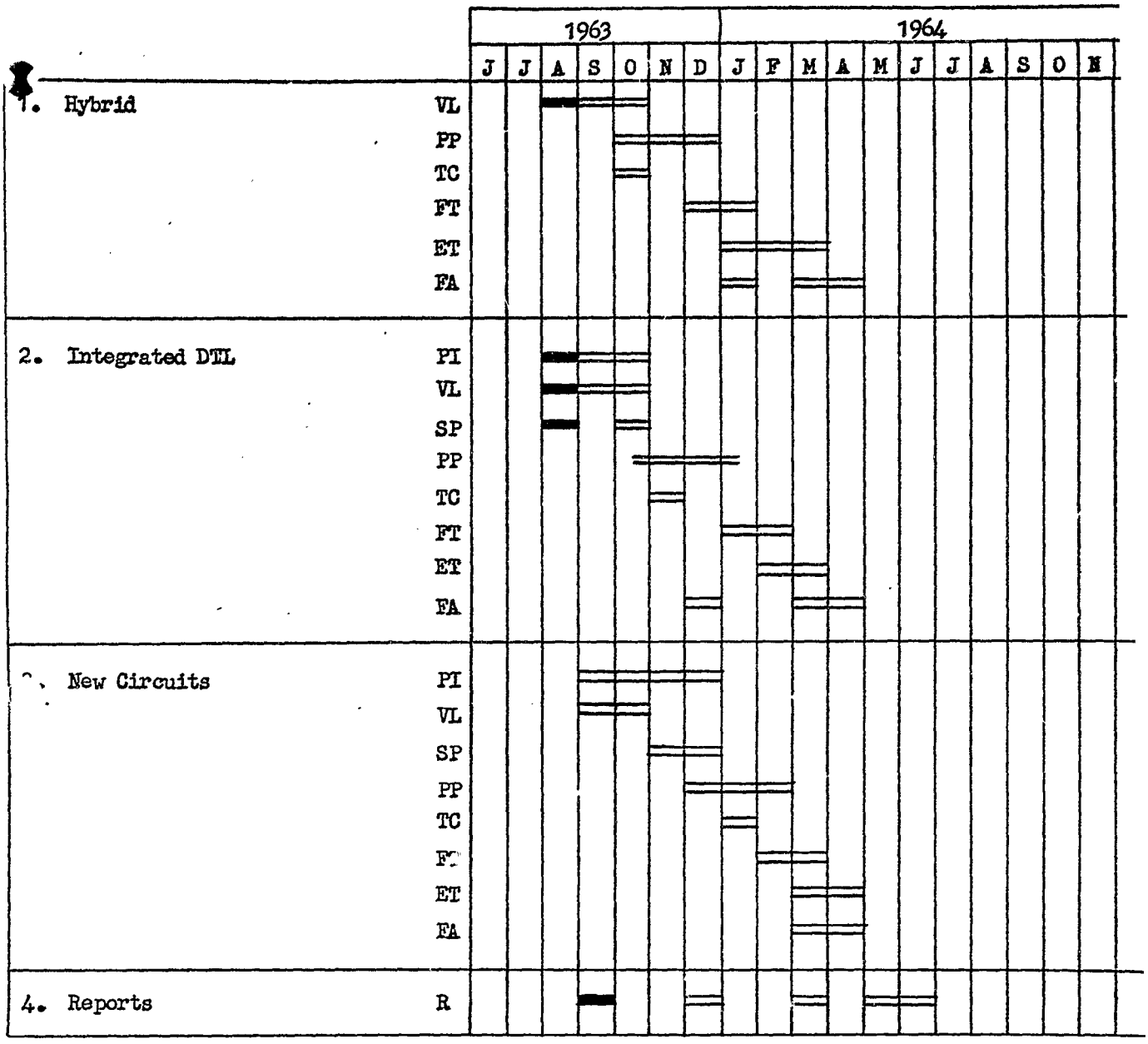


FIGURE 4. WAVESHAPES - INTEGRATED LOGIC CIRCUIT

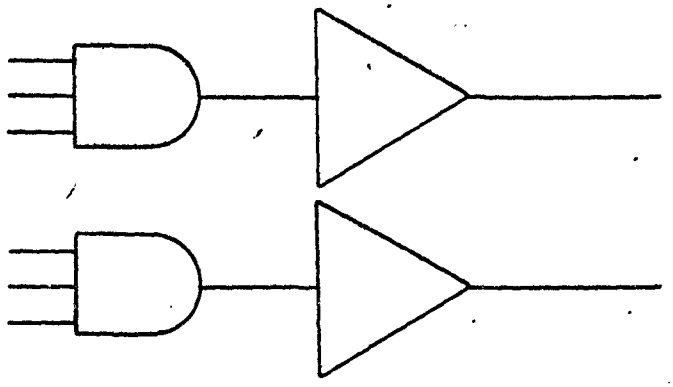


LEGEND

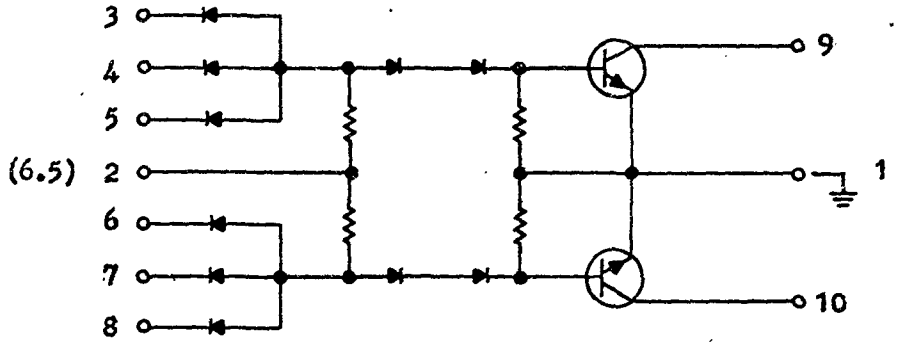
PI - Preliminary Investigation
VL - Vendor Liaison
SP - Specification Preparation
PP - Procurement
TC - Test Circuits
FT - Functional Test
ET - Environmental Test
FA - Failure Analysis
R - Reports
▬ - Work Schedule Complete
═ - Work Schedule Proposed

REV.

DWG. NO. 7900516



LOGIC SYMBOL



SCHEMATIC

RUU IDENT. NO.

TYPE			RRU CODE IDENT. NO.
CLASS		UNLESS OTHERWISE SPECIFIED (1) ALL DIMENSIONS ARE IN INCHES (2) TOLERANCES ARE DEC.: FRAC.: ANG.:	PURCHASED PART DRAWING
FIRST USER			Remington Rand Univac
DES. ENG.	DATE	TITLE: DIODE - TRANSISTOR GATE	DWG. NO. 7900516
COMP. ENG.	DATE		
QUALITY	DATE		
PDS	DATE	WEIGHT / CATALOGING CODE	SHEET 1 OF 8

I. APPLICABLE SPECIFICATIONS

MIL-23700 (Navy)

II. CONSTRUCTION AND DIMENSIONS (As shown in Figure 3)

III. PERFORMANCE CHARACTERISTICS (As shown in Table I)

Maximum Ratings:

P_D (Total)	Device Operating Above 25°C	R1 or R2 Dissipation	Resistor Derating	Temperature Range
200 mw	1.3 mw/°C	100 mw	0.67mw/°C	-65 to +175°C

IV. QUALITY ASSURANCE PROVISIONS

V	DWG NO 7900516	REV

TABLE I.

TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS
1. Visual & Mechanical					
2. Forward Current	$V_{2-3 \text{ thru } 8}$ = 6.5 Vdc V_{1-9} = 4.5 Vdc V_{1-10} = 4.5 Vdc V_{2-1} = 6.5 Vdc	$I_{2-3 \text{ thru } 8}$ I_{1-9} I_{1-10} I_{2-1}	5.2 3.2 3.2 6.6	6.4 4.4 4.4 11.0	mAdc mAdc mAdc mAdc
3. Reverse Current	$V_{3 \text{ thru } 8-2}$ = 4.5Vdc V_{1-2} = 4.5Vdc	$I_{3 \text{ thru } 8-2}$ I_{1-2}	— —	0.1 0.1	uAdc uAdc
4. Diode Effective Speed	See Figure 4 Connect 2 to C Connect 1 to D Alternately connect 3, 4, 5, 6, 7, 8 to B	$t_2 - t_1$		15	nsec
5. Saturation Voltage (Requires effective $h_{FE \text{ Min}} = 40$)	See Figure 5 Connect 1 to C Connect 2 to A Connect 3 thru 8 to +2.4 Vdc Alternately connect 9 and 10 to B	V_{9-1} (Sat) V_{10-1} (Sat)		0.35 0.35	Vdc Vdc

Remington Rand Univac
DIVISION OF SPERRY RAND CORPORATION

REVISIONS

DESCRIPTION	AUTH	DATE	COMP ENG	QUAL ASSURANCE	STD
REV LTR	IDENT NO	SHEET 3	V	DWG NO 7900516	

TABLE I. (Cont.)

TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS
6. Noise Rejection	See Figure 6 Connect 1 to C 2 to +A 9 to +B Alternately connect 3, 4, 5 to D	I_{9-1}	—	100	uAdc
	Connect 1 to C 2 to A 10 to B Alternately connect 6, 7, 8 to D	I_{10-1}	—	100	uAdc
7. Turn-On Time	See Figure 7 Connect 1 to C Connect 2 to +A R_c = 100 Ω				
	Alternately Supply Input to: 3, 4, 5 — GRD: 6, 7, 8 & 10 — B: 9	t_{On}		25	nsec
	Alternately Supply Input to: 6, 7, 8 — GRD: 3, 4, 5 & 9 — B: 10	t_{On}		25	nsec
8. Turn-Off Time	As Above	t_{off}		25	nsec
	Except R_c = 400 Ohms	t_{off}		25	nsec

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REVISIONS

SYM	AUTH	DESCRIPTION	DATE	COMP ENG	QUAL ASSURANCE	STD

RRU CODE IDENT NO

SHEET 4

DWG NO. 7900516

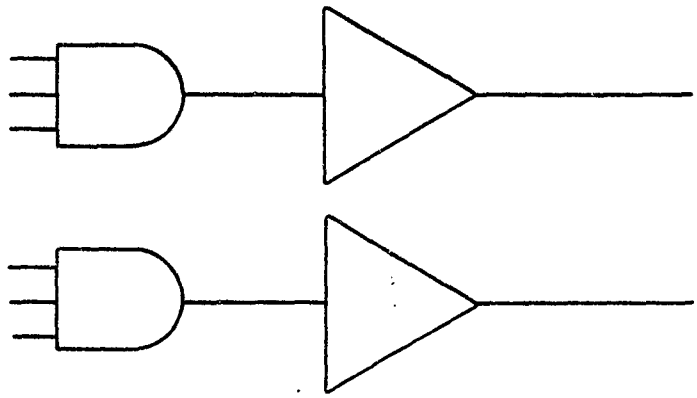

FIGURE 1. LOGIC DIAGRAM

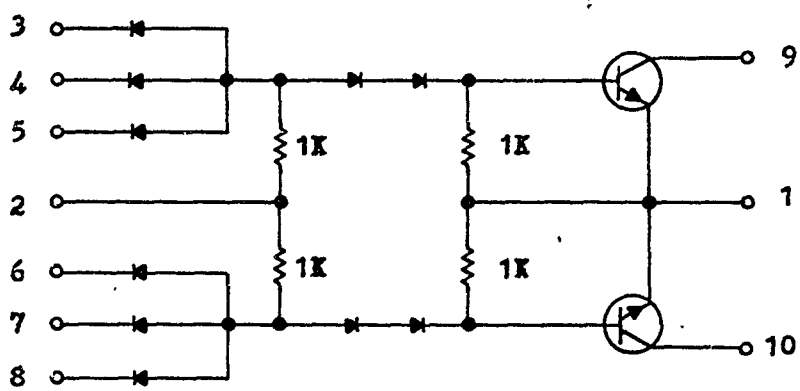

FIGURE 2. CIRCUIT SCHEMATIC

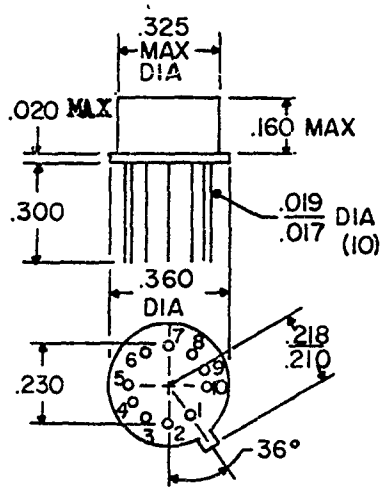

FIGURE 3. PHYSICAL DIMENSIONS

SYM	AUTH	DESCRIPTION	DATE	COMP ENG	QUAL ASSURANCE	STD

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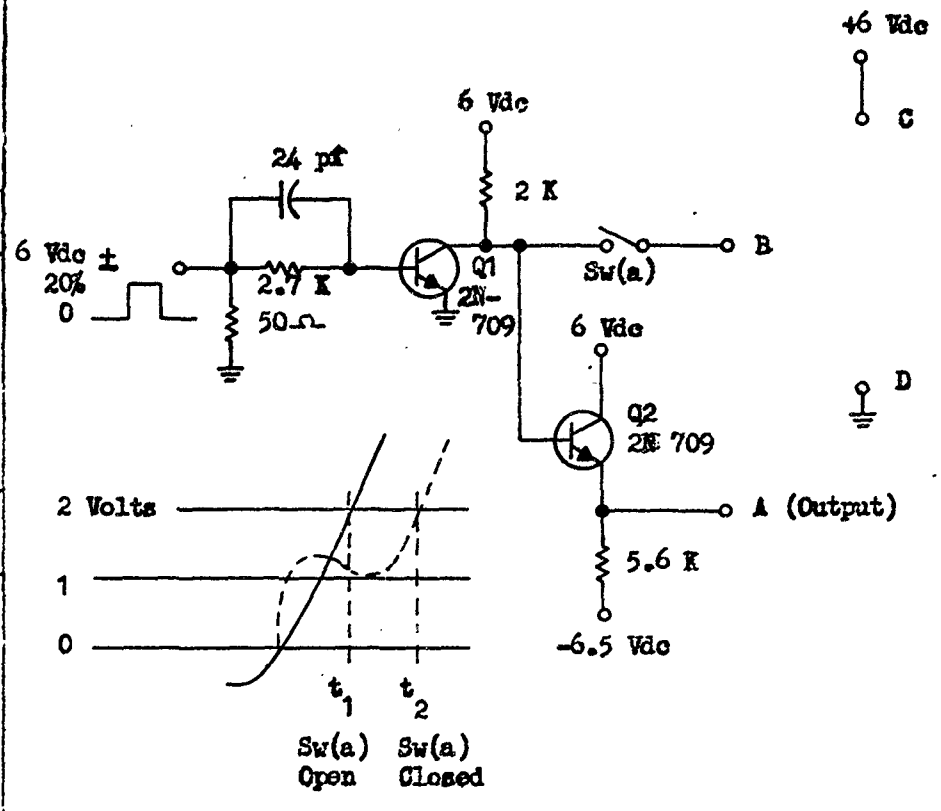
RRU CODE IDENT NO.	SHEET		DWG NO.
	5	V	7900516

A-1595



NOTES:

(1) Open Sw(a)
(2) Adjust Q1 for Q1 fall time which will result in output at Terminal A of 3 nanoseconds/volt positive slope for approximately 2.5 volts.
(3) Note t_1 (2 volt level)
(4) Close Sw(a)
(5) Note t_2 (2 volt level)

FIGURE 4. REVERSE RECOVERY TIME TEST CIRCUIT

SYM	AUTH	DESCRIPTION	DATE	COMP ENG	QUAL ASSURANCE	STD
		REVISIONS				

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RRU CODE IDENT NO.	SHEET		DWG NO.
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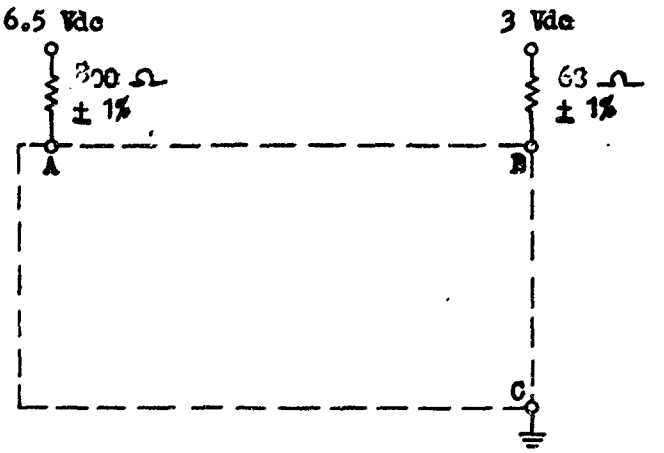


FIGURE 5. SATURATION VOLTAGE TEST CIRCUIT

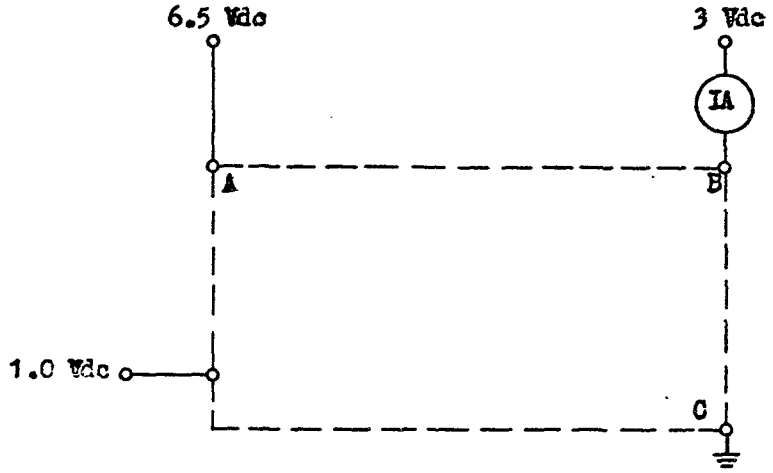


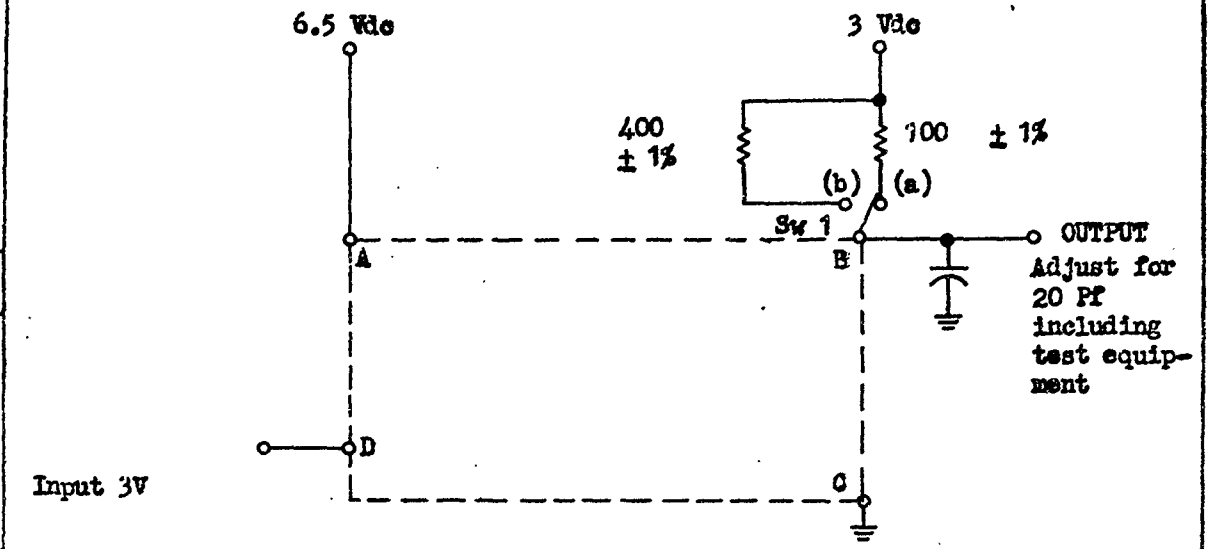
FIGURE 6. NOISE REJECTION TEST CIRCUIT

SYM	AUTH	DESCRIPTION	DATE	COMP ENG	QUAL ASSURANCE	STD

REVISIONS

Remington Rand Univac DIVISION OF SPERRY RAND CORPORATION	RRU CODE IDENT NO	SHEET 7	V	DWG NO. 7900516

A-1388



$t_r = t_f = 4$ nsec max.

FIGURE 7. TURN-ON (OFF) TIME TEST CIRCUIT

NOTES:

(1) Turn-on time for the above circuit is defined as the time interval from a point 10% up from the minimum amplitude on the leading edge of the input pulse to a point 90% down from the maximum amplitude on the leading edge of the output pulse.

(2) Turn-off time for the above circuit is defined as the time interval from a point 10% down from the maximum amplitude on the trailing edge of the input pulse to a point 50% down from the maximum amplitude on the trailing edge of the output pulse.

(3) Sw 1 in position (a) for Turn-On.

(4) Sw 1 in position (b) for Turn-Off.